

**INFORMATION DISCLOSURE STATEMENT PURSUANT TO
37 C.F.R. §§1.97-1.99**



PATENT APPLICATION

Applicant(s): Bryant, et al.

Docket No. BUR920010086US1

FOR: **FIN-BASED DOUBLE POLY
DYNAMIC THRESHOLD CMOS
FET WITH SPACER GATE AND
METHOD OF FABRICATION**

Serial No. 09/683,486

Filed: January 7, 2002

Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

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Sir:

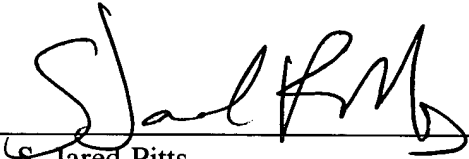
In accordance with the duty of disclosure under 37 C.F.R. §1.56 and pursuant to 37 C.F.R. §§1.97-1.99, Applicant(s) hereby notifies the U.S. Patent and Trademark Office of the documents listed on the attached Form PTO-1449. One copy of each cited document is submitted herewith. Applicant respectfully submits that all pending claims are patentable over the foregoing references, alone or in combination. The Examiner is requested to initial the enclosed Form PTO-1449 and return a copy thereof to the undersigned.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant reserves the right to dispute any of the listed documents as prior art during examination. Further, Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application. Furthermore, the submission of this Information Disclosure

Statement is not to be construed as a representation that a search has been made or that no other material information may exist.

This Information Disclosure Statement is being filed within three months of the filing date of the captioned patent application, and therefore no certification under 37 C.F.R. §1.97(e) or fee under 37 C.F.R. §1.17(p) is required.

Respectfully submitted,

By 
S. Jared Pitts
Reg. No.: 38,579

Date: November 9, 2001

Enclosures: PTO-1449
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